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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/612,222

07/03/2003

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300.1119

5751

21171 7590 11/24/2009

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EXAMINER

CHANG, RICK KILTAE

ART UNIT

PAPER NUMBER

3726

MAIL DATE

DELIVERY MODE

11/24/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/612,222	<b>Applicant(s)</b> AKAGAWA ET AL.	
	<b>Examiner</b> Rick K. Chang	<b>Art Unit</b> 3726	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13, 15, 17, 19-31, 33, 35, 49 and 50 is/are pending in the application.
- 4a) Of the above claim(s) that are not listed in item 6 below is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 7, 8, 11-13, 15, 17, 19, 20, 25, 26, 29-31, 33, 35 and 49 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/30/09</u> .   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Drawings***

1. The drawing was received on 7/8/09. This drawing is approved.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The disclosure, as originally filed, failed to provide support for “forming via holes . . . maximum value” and “a wiring board”.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35, 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There are numerous phrases and clauses in the claims that are vague, indefinite, and/or awkwardly and confusingly worded, and therefore, are not fully understood. The following are examples:

Art Unit: 3726

Claim 1, lines 1-3: Is "a component-embedded board" referring to "a wiring board" or something else? There is no support for "a wiring board".

Claim 1, line 4: Is "said board" referring to "a component-embedded board," "a wiring board" or something else?

Claims are ambiguous and competitors would be unable to discern the bounds of the invention.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35 and 49, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Taff et al (US 6,165,658) in view of Leedy (US 5,103,557).

Re claims 1, 4, 19 and 22: Taff discloses detecting, before a wiring board is covered with a first insulating layer, the actual position of a first electronic component formed on a surface of said board (col. 7, lines 22-57 and col. 8, lines 55-58, entire cols. 14-16); calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data (col. 8, lines 58-65, entire cols. 14-16); determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective (12 and 24 in Fig. 1; col. 7, lines 66-67

Art Unit: 3726

and col. 8, lines 1-5 and col. 8, lines 5-45); correcting, based on said first displacement data, design data to be used for processing said board, covering said board with said first insulating layer to form a wiring pattern connected to said first electrical component (col. 8, lines 5-67 and col. 9, lines 1-2); and forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer (col. 7, lines 22-57 and col. 8, lines 44-54, entire cols. 14-16); discloses if the represented displacement does exceed the predetermined maximum value, performing no corrections to the design data (col. 8, lines 46-54; 12 and 24 in Fig. 1; col. 7, lines 66-67 and col. 8, lines 1-5, entire cols. 14-16), except for detecting is performed before a first insulating layer covers the board.

Leedy discloses detecting is performed before a first insulating layer covers the board (in Fig. 5, there is no insulating layer between 15-1 and 2-1 as well as 15-2 to 2-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Taff by detecting is performed before a first insulating layer covers the board, as taught by Leedy, for the purpose of determining the positions of the electronic components.

Re claims 2 and 20: Taff discloses applying, based on said design data corrected in said correcting, a maskless exposure to the board covered with said first insulating layer (col. 9, lines 12-26).

Art Unit: 3726

Re claims 7-8, 11-12, 25-26 and 29-30: Taff discloses applying, based on said design data corrected in said correcting, based on said second displacement data, a maskless exposure to said board covered with said second insulating layer (col. 9, lines 12-26).

Re claims 13, 15, 17, 31, 33 and 35: Taff discloses that when the actual position of a terminal of the formed electronic component is displaced from an end of a wiring line that is defined in the design data as being the end to be connected to the terminal of the electronic component (col. 8, lines 55-63; for example, in Fig. 1, a wiring between terminals 10 and 12 connects to terminal 14 instead of connecting to terminal 12 as defined in the design data), the correcting, based on the second displacement data (displacement between the actual and the design data), corrects the design data so as to move the end of the wiring line to be connected to the terminal of the electronic component to the actual position of the formed electronic component (col. 10, lines 14-17; redirecting the wiring between terminals 10 and 14 to terminals 10 and 12).

Claim 49: Taff discloses in col. 17, lines 12-20 calculating correction file relative to a CAD reference (means for calculating a displacement; a CPU of a computer) and implementation of the correction (means for correcting; a CPU of a computer); means for determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective (12 and 24 in Fig. 1; col. 7, lines 66-67 and col. 8, lines 1-5 and col. 8, lines 5-45; a CPU of a computer); if the represented displacement does not exceed the predetermined maximum value (col. 8, lines 5-45), correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to

Art Unit: 3726

said first electrical component (col. 8, lines 65-67 and col. 9, lines 1-2); and forming via holes in the first insulating layer in accordance with the corrected design data, thereby compensating for the actual location of the displaced first electronic component in a subsequent layer (col. 7, lines 22-57 and col. 8, lines 44-54); discloses if the represented displacement does exceed the predetermined maximum value, performing no corrections (col. 8, lines 46-63; 12 and 24 in Fig. 1; col. 7, lines 66-67 and col. 8, lines 1-5), except for means for detecting.

Leedy discloses in Fig. 5 means for detecting (10, 36, 46, 48, 50, 38, 40, 15-1, 15-2 . . .).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Taff by detecting is performed before a first insulating layer covers the board, as taught by Leedy, for the purpose of determining the positions of the electronic components.

### ***Response to Arguments***

8. Applicant's arguments filed 7/8/09 have been fully considered but they are not persuasive.

The disclosure failed to provide support that during the forming via holes the determination is made whether the represented displacement does not exceed the predetermined max. value or not. Further, there is no support that the via holes are formed "only if the . . ." As stated in the specification, Page 11, line 15, the determination of whether the board is defective or not is performed prior to forming the via holes. Furthermore, the step of determining whether exceeded the max. value or not is performed twice in the claim, which is not support by the specification (claim 1, lines 9-10 and 14-15).

Art Unit: 3726

12 and 24 in Fig. 1; col. 7, lines 66-67 and col. 8, lines 1-5 and col. 8, lines 5-45 discloses the step of determining whether the displacement value exceeds the predetermined maximum value. Specifically, the predetermined max. value is “any post or pin centered on conductive site 24 with a diameter which is at least as great as the diameter of conductive site 24 would make electrical contact between 24 and 12 by penetrating both the first inner layer 4 and 6. Anything outside of this would be defective.

Fig. 1 clearly shows a step of covering the board with the first insulating layer to form a wiring pattern. It is noted that the features upon which applicant relies (i.e., the covering and forming are also performed only when the displacement value does not exceed the predetermined max. value) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

### ***Interviews After Final***

9. Applicant note that an interview after a final rejection must be submitted briefly in writing the intended purpose and content of the interview (the agenda of the interview must be in writing). Upon review of the agenda, the Examiner may grant the interview if the examiner is convinced that disposal or clarification for appeal may be accomplished with only nominal further consideration. Interviews merely to restate arguments of record or to discuss new limitations will be denied. See MPEP 714.13 and 713.09.

### ***Conclusion***

10. Please provide reference numerals (either in parentheses next to the claimed limitation or in a table format with one column listing the claimed limitation and another column listing



Art Unit: 3726

corresponding reference numerals in the remark section of the response to the Office Action) to all the claimed limitations as well as support in the disclosure for better clarity (optional).

Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (571) 272-4564. The examiner can normally be reached on 5:30 AM to 1:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Bryant can be reached on (571) 272-4526. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 3726

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rick K. Chang/  
Primary Examiner, A.U. 3726

RC  
November 23, 2009